FUTUR-IC: A Sustainable Microchip Manufacturing Alliance

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Overview

For the first time in more than 40 years, the semiconductor microchip industry is confronted with limits to transistor size, to its environmental footprint, and to its workforce pipeline readiness. With the National Science Foundation Convergence Accelerator program, we have established a global microchip sustainability alliance called FUTUR-IC, driving the convergence of Technology-Ecology-Workforce (TEW) in a three-dimensional (3D) fashion to establish a common ground for "green" business.

Description

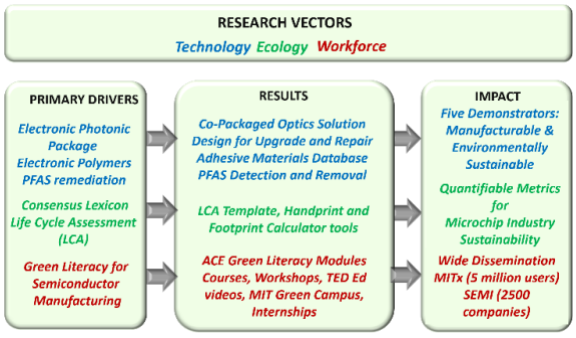

Figure 1. Holistic roadmap to build consensus across the microchip supply chain through a global alliance.

Microchip manufacturing and systems can be traced to 31% of global greenhouse gas emissions today. Mega Data Centers consuming tens of Megawatts of power and growing at 25-30% per year driven by video demand, will require 10% of the world electricity generation by 2030. Regulatory solutions threaten to disrupt the economics of an efficient global supply chain. Technology solutions require synchronized innovation along the supply chain from materials suppliers to system integrators to end users. FUTUR-IC supports continued scaling of system performance while targeting Net Zero environmental impact by 2050 for the global community.

Semiconductor hardware, software and system architectures are undergoing simultaneous technology transitions today that present both opportunities and uncertainties. The information systems that drive Data Center workflows and ubiquitous sensing installations for the Internet of Things (IoT) aim to do the impossible: scale down costs, energy consumption, and latency to nearly zero, while simultaneously amplifying bandwidth and connectivity to seemingly infinite levels, within a constrained environmental envelope. Solutions defined by concurrent TEW constraints will build converged pathways on which to base decades of progress. The time to surmount these roadblocks for the microchip industry is *now*!

Differentiators

FUTUR-IC Global Alliance is a member-led association of thought leaders from industry, academia, and government working together to assess and remedy common risks presented by technology change, ecology boundaries, and workforce competency. *This unique Alliance creates consensus for investments with its 3D-TEW research model.* FUTUR-IC accelerates convergence of materials science with life-cycle analysis to drive materials and process design towards sustainable production and products.

Road Map

Technology: FUTUR-IC has adopted electronic-photonic package integration as its hardware

driver. It has targeted scaling chip package Input-Output (I/O) to > 1 Petabit/second within a Net Zero ecology envelope. Investment examples are: 1) PFAS-free materials and process flows to meet package scaling requirements; 2) adhesive materials database for low temperature assembly; and 3) demonstration of new chip package architectures that mitigate end-of-life waste with capability for repair and upgrade under a new Design for Upgrade, Repair, Reduce, Reuse, Recycle (DfUR[4]) initiative.

Ecology: FUTUR-IC will 1) create data analytics for environmental and social impacts of microchip product lifecycles; 2) develop a consensus set of figures of merit; 3) develop the tools and processes for timely Life Cycle Assessment (LCA); 4) provide data and analysis for a guidance roadmap; and 5) provide tools for decreasing *footprint burdens and increasing handprint remediations*. (The handprint is an innovative and holistic approach to facilitate the measurement, evaluation, and communication of the ecological, economic and social sustainability impacts of products).

Workforce: FUTUR-IC provides a multidimensional TEW awareness that is transformed into solutions by its new educational curricula and content. Examples are: 1) SEMI (the microchip supply chain consortium) Green Literacy programs, 2) summer schools and bootcamps, 3) university courses, 4) Problem Based Learning (PBL) for community colleges, 5) TED-Ed videos and Virtual Reality (VR) sustainability games for K-to-Gray learners, 6) two MIT green campus demonstrator sites for e-waste mitigation and green manufacturing materials and processes, 7) full spectrum internships for high school and community college students, and 8) annual workforce needs reports for each participating community.

Partnerships

FUTUR-IC's partners have developed programs across all three TEW vectors. Examples are Technology: **iNEMI** (industry association for joint development projects) for adhesive package materials; Ecology: tools and processes for LCA and handprinting throughout the **microchip supply chain**; Workforce: **SEMI** sustainability literacy for executives and incumbent workers.

Figure 2. Current FUTUR-IC Partners

Intellectual Property

FUTUR-IC has filed three patents for assembly and architecture for advanced packaging. Continued IP development is governed by three agreements: 1) shared rights under MIT's Industrial Consortium; 2) exclusive rights under negotiated research agreements; and 3) Joint Development Project rights under standard iNEMI protocols.

The Package Scaling Era

The Chip Scaling Era has ended, and the Package/System Scaling Era is now in full implementation with **no long-term technology roadmap**. To maintain performance scaling: i) incremental technology change is insufficient, and ii) supply chain sustainability in terms of workforce quality, materials criticality, and manufacturing effluent has no inherent scaling vector. Economic risk for the nation has never been so large, and rarely been so dependent on a particular technology evolution.

This transformation to chip/package scaling is not a task that any one sector can tackle in isolation; it requires a robust global alliance that unites academia, industry, government, and community. FUTUR-IC offers such a collective effort to pave the way for innovative solutions, ensuring a resilient and prosperous technological future.